MAX V CPLD Development Board

Reference Manual

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MNL-01061-1.1

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QUALITY
ISO 9001:2008
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Contents

1. Overview

Introduction

This document describes the hardware features of the MAX® V CPLD development board, including the detailed pin-out and component reference information required to create custom CPLD designs that interface with all components of the board.

General Description

The MAX V CPLD development board provides a hardware platform for developing and prototyping low-cost, low-power CPLD designs, as well as to demonstrate the features of the MAX V CPLD device.

To facilitate the development of MAX V CPLD designs, the board provides connectors to interface to external functions or devices.

For more information on the MAX V CPLD device family, refer to the *MAX V Device Handbook*.

Board Component Blocks

The board features the following major component blocks:

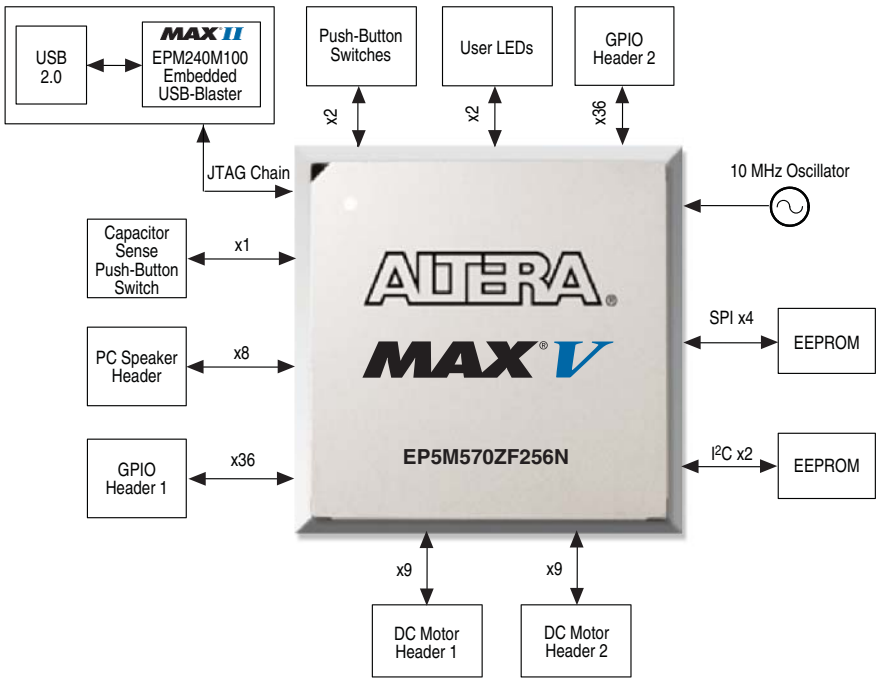
- MAX V CPLD 5M570ZF256C5N in a 256-pin FineLine BGA (FBGA) package
  - 570 logic elements (LEs)
  - 440 equivalent macrocells
  - 8,192-bits user flash memory (UFM)
  - 4 global clocks
  - 159 user I/Os
  - 1.8-V core power
- MAX II EPM240M100C4N CPLD in the 100-pin Micro FBGA (MBGA) package
- On-Board configuration circuitry
  - Embedded USB-Blaster™ for use with the Quartus® II Programmer
- On-Board connectors
  - Type-B USB connector (as power source and communication port)
  - Two general purpose I/O (GPIO) 2×20-pin 0.1-inch expansion headers
  - One 4-pin PC speaker header
  - Two 2×3-pin DC motor headers
- On-Board clocking circuitry
  - 10-MHz single-ended external oscillator

- General user I/O
  - LEDs and display
    - Two CPLD user LEDs
    - One USB status LED
    - One power status LED
  - Push-Button switches
    - Two user-defined push-button switches
    - One capacitor sense push-button switch
- Mechanical
  - 4.1″ × 3.1″ board

Development Board Block Diagram

Figure 1–1 shows the block diagram of the MAX V CPLD development board.

Figure 1–1. MAX V CPLD Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

Introduction

This chapter introduces the major components on the MAX V CPLD development board. Figure 2–1 illustrates major component locations and Table 2–1 provides a brief description of all component features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the MAX V CPLD development kit documents directory.

For information about powering up the board and installing the demonstration software, refer to the *MAX V CPLD Development Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the MAX V CPLD development board, including an annotated board image and component descriptions. Figure 2–1 provides an overview of the development board features.

Figure 2–1. Overview of the MAX V CPLD Development Board Features

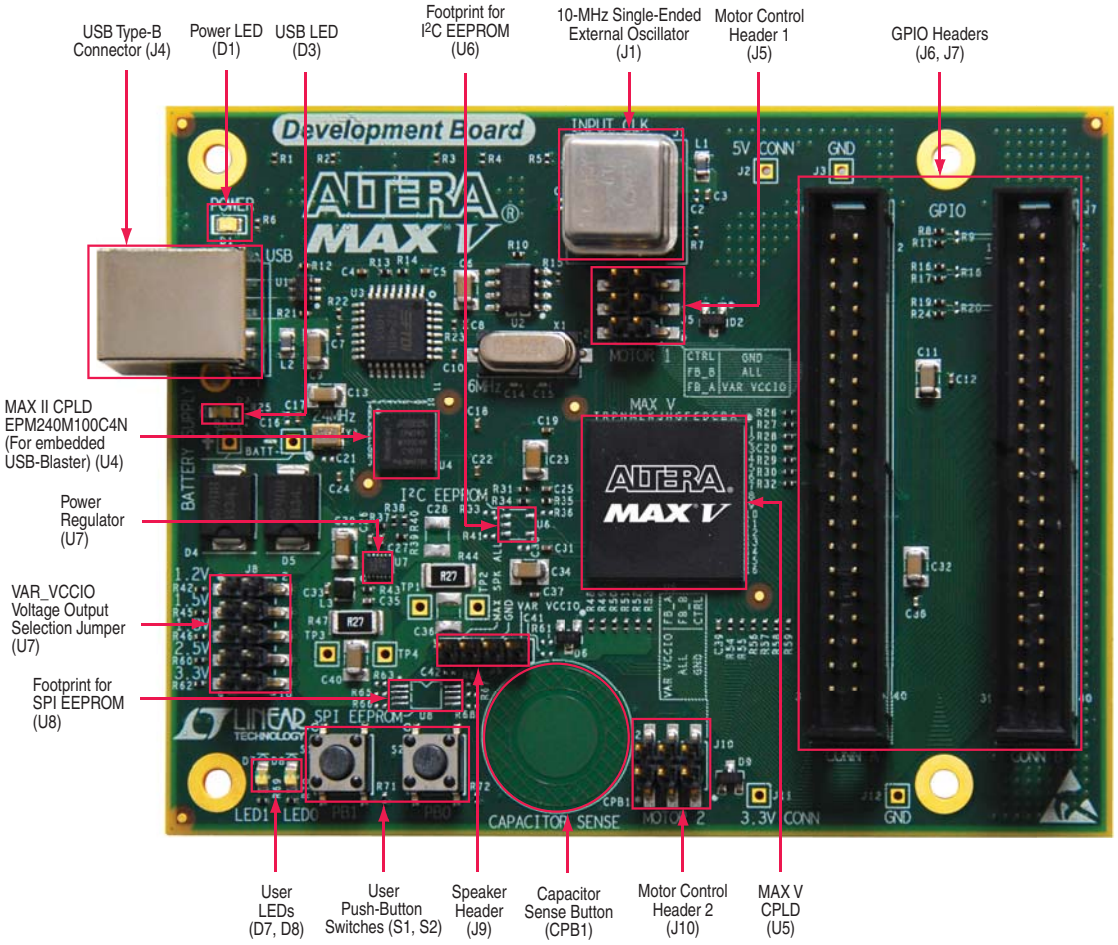


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. MAX V CPLD Development Board Components (Part 1 of 2)

Board Reference	Type	Description
Featured Device		
U5	CPLD	MAX V 5M570ZF256C5N, 256-pin FBGA.
Configuration, Status, and Setup Elements		
J4	USB Type-B connector	Connects the USB cable to the computer to enable embedded USB-Blaster JTAG. The connector also supplies power to the board through a USB cable when the cable is connected to a PC USB slot at the other end.

Table 2–1. MAX V CPLD Development Board Components (Part 2 of 2)

Board Reference	Type	Description
U3	USB 2.0 PHY	A FTDI USB 2.0 PHY device to configure the CPLD over embedded USB-Blaster.
U4	CPLD	MAX II CPLD EPM240M100.
J13, J14	JTAG header	Footprint (at the bottom of the board) to mount a JTAG header. The header allows direct-access to devices in the JTAG connection.
D1	Power LED	Illuminates when 5-V USB power is present.
D3	USB LED	Illuminates to indicate USB-JTAG activity.
Clock Circuitry		
J1	10-MHz oscillator	10-MHz single-ended input clock for the MAX V CPLD.
X1	6-MHz oscillator	6-MHz input clock for the FTDI USB 2.0 PHY device.
Y1	24-MHz oscillator	24-MHz input clock for the MAX II CPLD EPM240M100.
Connectors		
J6, J7	GPIO headers	Two general-purpose 2x40-pin 0.1-inch expansion headers.
J9	PC speaker header	A 4-pin PC speaker header which connects to the MAX V CPLD I/O bank 2.
J5, J10	DC motor headers	Two motor headers which connects to the MAX V CPLD I/O bank 2.
General User Input/Output		
D7, D8	User LEDs	Two user LEDs. Illuminates when driven low.
S1, S2	User push-button switches	Two user push-button switches. Driven low when pressed.
CPB1	Capacitor sense button	One capacitive touch-sense user-defined button.
Off-Chip EEPROM		
U6	I^2C EEPROM	Footprint to install an I^2C serial EEPROM
U8	SPI EEPROM	Footprint to install a SPI EEPROM.

Featured Device: MAX V CPLD

The MAX V CPLD development board features the MAX V CPLD 5M570ZF256C5N device (U5) in a 256-pin FBGA package.

Table 2–2 describes the features of the MAX V CPLD 5M570ZF256C5N device.

Table 2–2. MAX V CPLD 5M570ZF256C5N Device Features

Equivalent LEs	User Flash Memory (bits)	User I/Os	Global Clocks	Package Type
570	8192	159	4	256-pin FBGA

For more information about MAX V CPLD device family, refer to the *MAX V Device Handbook*.

Table 2–3 lists the MAX V CPLD device component reference and manufacturing information.

Table 2–3. MAX V CPLD Device Component Reference and Manufacturing Information

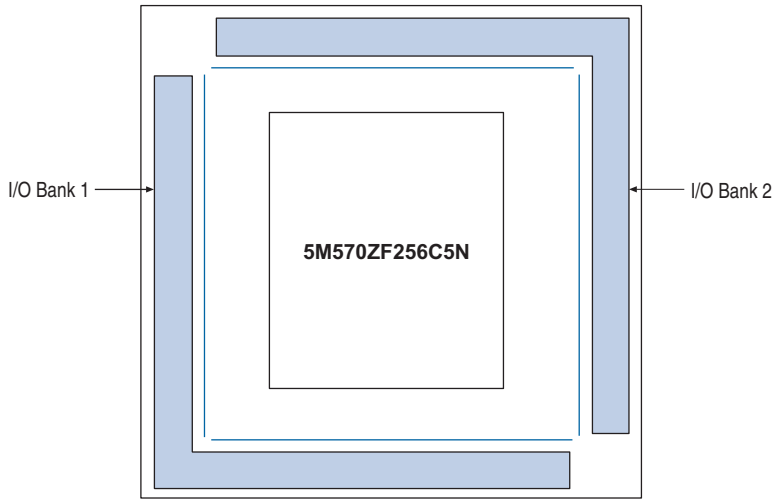
Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U5	MAX V CPLD, 256-pin FBGA package, 570 LEs, lead-free.	Altera Corporation	5M570ZF256C5N	www.altera.com

I/O Resources

The 5M570ZF256C5N device support two I/O banks and each of these banks support all the LVTTL, LVCMOS, LVDS, and RSDS standards.

Figure 2–2 illustrates the bank organization for the 5M570ZF256C5N device in a 256-pin FBGA package.

Figure 2–2. 5M570ZF256C5N Device I/O Bank Diagram *(Note 1)*



Note to Figure 2–2:

(1) This figure is a top view of the silicon die and is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Table 2–4 lists the MAX V CPLD device pin count and usage by function on the development board.

Table 2–4. MAX V CPLD Device I/O Pin Count and Usage (Part 1 of 2)

Function	I/O Standard	I/O Count	Special Pins
40-pin GPIO Header A	3.3-V CMOS	36	—
40-pin GPIO Header B	1.2-V to 3.3-V	36	—
PC Speaker Header		8	—
DC Motor Headers		18	—

Table 2–4. MAX V CPLD Device I/O Pin Count and Usage (Part 2 of 2)

Function	I/O Standard	I/O Count	Special Pins
Push-Buttons	3.3-V CMOS	2	Push-button 2: `Dev_CLRn`
User LEDs		2	—
I^2C EEPROM		2	—
SPI EEPROM		4	—
Clock		1	—
Device I/O Total:		109/159	

Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements.

Configuration

The MAX V CPLD development board supports the following device configuration methods:

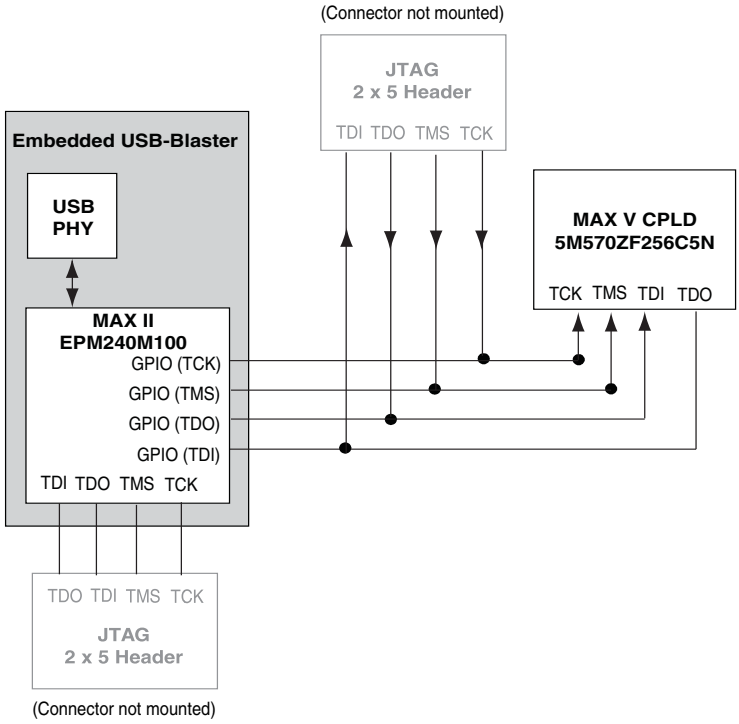
- Embedded USB-Blaster is the default method for configuring the CPLD at any time using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- External USB-Blaster for configuring the CPLD using a JTAG connector. To use this optional method to configure the CPLD, you have to mount the JTAG connector or header to the back of the board.

CPLD Configuration over Embedded USB-Blaster

The USB-Blaster is implemented using a USB Type-B connector (J4), a FTDI USB 2.0 PHY device (U3), and an Altera MAX II CPLD EPM240M100 (U4). This allows the configuration of the MAX V CPLD using a USB cable which connects between the USB port on the board (J4) and a USB port of a PC running the Quartus II software. The JTAG chain is normally mastered by the embedded USB-Blaster found in the MAX II CPLD EPM240M100.

Figure 2–3 illustrates an exmaple of the JTAG chain connection.

Figure 2–3. JTAG Chain



The primary configuration mode for the MAX V CPLD is via JTAG using the MAX II configuration controller design (embedded USB-Blaster). The board also includes a JTAG connector which interfaces directly to the MAX V CPLD as the alternate source for configuration.

CPLD Configuration using External USB-Blaster

The JTAG programming header (J13) provides another method for configuring the CPLD using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster connects to the board through the JTAG connector. Figure 2–3 illustrates the JTAG chain.

Status Elements

This section describes the status elements. The development board includes two status LEDs which connects to the MAX V CPLD.

Table 2–5 lists the LED board references, names, and functional descriptions.

Table 2–5. Board-Specific LEDs

Board Reference	LED Name	Description
D1	Power	Blue LED. Illuminates when power is active.
D3	USB	Green LED. Illuminates when the embedded USB-Blaster is in use. Driven by the MAX II CPLD EPM240M100.

Table 2–6 lists the board-specific LEDs component references and manufacturing information.

Table 2–6. Board-Specific LEDs Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D1	Blue LED	Lite-On	LTST-C170TBKT	www.liteon.com
D3	Green LEDs	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com

Setup Elements

The development board does not have any setup elements.

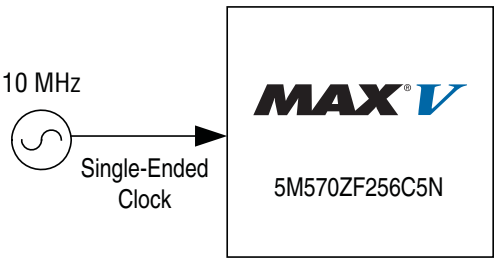
To power-up the board, ensure that the VAR_VCCIO jumper is set to 3.3 V before plugging the USB cable into the USB Type-B connector (J4).

Clock Circuitry

The development board includes a single-ended clock input on a 4-pin through-hole socket. To replace the clock input with a different frequency oscillator, unplug the current oscillator from the board and plug the desired oscillator into the 4-pin socket.

Figure 2–4 shows the MAX V CPLD development board clock input.

Figure 2–4. MAX V CPLD Development Board Clock Input



The development board also includes a 6-MHz crystal oscillator which provides the input clock for the USB 2.0 PHY device.

Table 2–16 lists the oscillator component reference and the manufacturing information.

Table 2–7. Oscillator Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J1	10-MHz oscillator, 3.3 V, CMOS, 12.7 mm × 12.7 mm, 1/2-SZ, ±30 ppm.	Abracon Corporation	ACHL-10.000MHZ-EK	www.abracon.com
X1	6-MHz crystal oscillator, 20pF SMD.	CTS Corporation	ATS060SM-T	www.ctscorp.com
Y1	24-MHz oscillator, 3.3 V, CMOS SMD 3.2 mm × 2.5 mm, ±50 ppm.	Abracon Corporation	ASE-24.000MHZ-ET	www.abracon.com

Connectors

This section describes the connectors available on the development board.

GPIO Headers

There are two general-purpose 2×20-pin 0.1-inch expansion headers to allow the addition of daughtercards for supplementary board features and functions.

Table 2–15 lists the GPIO header A schematic signal names and their corresponding MAX V CPLD device pin numbers.

Table 2–8. GPIO Header A Schematic Signal Names and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
J6.1	GPIO connector A pin	AGPIO_1	3.3-V	P2
J6.2	GPIO connector A pin	AGPIO_2		M4
J6.3	GPIO connector A pin	AGPIO_3		L4
J6.4	GPIO connector A pin	AGPIO_4		N3
J6.5	GPIO connector A pin	AGPIO_5		N2
J6.6	GPIO connector A pin	AGPIO_6		N1
J6.7	GPIO connector A pin	AGPIO_7		M3
J6.8	GPIO connector A pin	AGPIO_8		M2
J6.9	GPIO connector A pin	AGPIO_9		M1
J6.10	GPIO connector A pin	AGPIO_10		L3
J6.11	Power	5VIN_CONN	5-V	—
J6.12	Ground	GND	—	—
J6.13	GPIO connector A pin	AGPIO_11	3.3-V	L1
J6.14	GPIO connector A pin	AGPIO_12		L2
J6.15	GPIO connector A pin	AGPIO_13		K2
J6.16	GPIO connector A pin	AGPIO_14		K3
J6.17	GPIO connector A pin	AGPIO_15		J3
J6.18	GPIO connector A pin	AGPIO_16		K1
J6.19	GPIO connector A pin	AGPIO_17		J1
J6.20	GPIO connector A pin	AGPIO_18		J2
J6.21	GPIO connector A pin	AGPIO_19		H2
J6.22	GPIO connector A pin	AGPIO_20		H3
J6.23	GPIO connector A pin	AGPIO_21		G3
J6.24	GPIO connector A pin	AGPIO_22		H1
J6.25	GPIO connector A pin	AGPIO_23		G1
J6.26	GPIO connector A pin	AGPIO_24		G2
J6.27	GPIO connector A pin	AGPIO_25		F2
J6.28	GPIO connector A pin	AGPIO_26		F3
J6.29	Power	3.3VIN_CONN		—
J6.30	Ground	GND	—	—

Table 2–8. GPIO Header A Schematic Signal Names and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
J6.31	GPIO connector A pin	AGPIO_27	3.3-V	E3
J6.32	GPIO connector A pin	AGPIO_28		F1
J6.33	GPIO connector A pin	AGPIO_29		E1
J6.34	GPIO connector A pin	AGPIO_30		E2
J6.35	GPIO connector A pin	AGPIO_31		D2
J6.36	GPIO connector A pin	AGPIO_32		D3
J6.37	GPIO connector A pin	AGPIO_33		C3
J6.38	GPIO connector A pin	AGPIO_34		D1
J6.39	GPIO connector A pin	AGPIO_35		E4
J6.40	GPIO connector A pin	AGPIO_36		C2

Table 2–15 lists the GPIO header B schematic signal names and their corresponding MAX V CPLD device pin numbers.

Table 2–9. GPIO Header B Schematic Signal Names and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
J7.1	GPIO connector B pin	BGPIO_P_1_R	Variable VCCIO voltage (1.2-V to 3.3-V)	D15
J7.2	GPIO connector B pin	BGPIO_P_2_R		D16
J7.3	GPIO connector B pin	BGPIO_N_1_R		C14
J7.4	GPIO connector B pin	BGPIO_N_2_R		C15
J7.5	GPIO connector B pin	BGPIO_P_3_R		E15
J7.6	GPIO connector B pin	BGPIO_7		B14
J7.7	GPIO connector B pin	BGPIO_N_3_R		D13
J7.8	GPIO connector B pin	BGPIO_8		C12
J7.9	GPIO connector B pin	BGPIO_9		E16
J7.10	GPIO connector B pin	BGPIO_10		E14
J7.11	Power	5VIN_CONN		—
J7.12	Ground	GND		—
J7.13	GPIO connector B pin	BGPIO_11		F13
J7.14	GPIO connector B pin	BGPIO_12		F16
J7.15	GPIO connector B pin	BGPIO_13		F15
J7.16	GPIO connector B pin	BGPIO_14		F14
J7.17	GPIO connector B pin	BGPIO_15		G16
J7.18	GPIO connector B pin	BGPIO_16		G15
J7.19	GPIO connector B pin	BGPIO_17		G14
J7.20	GPIO connector B pin	BGPIO_18		H16
J7.21	GPIO connector B pin	BGPIO_19		H15
J7.22	GPIO connector B pin	BGPIO_20		H14
J7.23	GPIO connector B pin	BGPIO_21		J16

Table 2–9. GPIO Header B Schematic Signal Names and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
J7.24	GPIO connector B pin	BGPIO_22	Variable VCCIO voltage (1.2-V to 3.3-V)	J15
J7.25	GPIO connector B pin	BGPIO_23		J14
J7.26	GPIO connector B pin	BGPIO_24		K16
J7.27	GPIO connector B pin	BGPIO_25		K15
J7.28	GPIO connector B pin	BGPIO_26		K14
J7.29	Power	3.3VIN_CONN	3.3-V	—
J7.30	Ground	GND	—	—
J7.31	GPIO connector B pin	BGPIO_27	Variable VCCIO voltage (1.2-V to 3.3-V)	L16
J7.32	GPIO connector B pin	BGPIO_28		L15
J7.33	GPIO connector B pin	BGPIO_29		L14
J7.34	GPIO connector B pin	BGPIO_30		M16
J7.35	GPIO connector B pin	BGPIO_31		M15
J7.36	GPIO connector B pin	BGPIO_32		M14
J7.37	GPIO connector B pin	BGPIO_33		L13
J7.38	GPIO connector B pin	BGPIO_34		M13
J7.39	GPIO connector B pin	BGPIO_35		N14
J7.40	GPIO connector B pin	BGPIO_36		N13

Table 2–16 lists the GPIO headers component reference and the manufacturing information.

Table 2–10. GPIO Headers Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J6, J7	GPIO headers	JMSCONN Technology	217040SE	www.jmsconn.com

PC Speaker Header

The development board includes one PC speaker header which connects to the MAX V CPLD I/O bank 2. The speaker header also supports a compatible standard four-pin motherboard speaker.

Table 2–15 lists the speaker header schematic signal names and their corresponding MAX V CPLD device pin numbers.

Table 2–11. Speaker Header Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
J9.1	Speaker header I/O pin	MAX_SPK_0	Variable VCCIO voltage (1.2-V to 3.3-V)	N15
	Speaker header I/O pin	MAX_SPK_1		N16
	Speaker header I/O pin	MAX_SPK_2		P15
	Speaker header I/O pin	MAX_SPK_3		P14
	Speaker header I/O pin	MAX_SPK_4		H12
	Speaker header I/O pin	MAX_SPK_5		J12
	Speaker header I/O pin	MAX_SPK_6		A8
	Speaker header I/O pin	MAX_SPK_7		A7
J9.4	Power	VAR_VCCIO		—
J9.3	Ground	GND	—	—

Table 2–16 lists the speaker header component reference and the manufacturing information.

Table 2–12. Speaker Header Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J9	0.025 inches (0.64 mm) square post header	Samtec	TSW-104-07-G-S	www.samtec.com
—	4-pin, 2-wire motherboard speaker *(1)*	Pc Parts Collection	20503	www.pcpartscollection.com

Note to Table 2–12:

(1) This component is a compatible unit which can be used on the development board. The MAX V CPLD development kit does not include this component.

DC Motor Headers

The development board includes two DC motor headers which are driven by six open-drain I/Os from the MAX V CPLD. The headers can directly drive micro DC motor and also provides two channels for DC motor encoder to measure the motor's rotation speed.

Table 2–15 lists the motor headers schematic signal names and their corresponding MAX V CPLD device pin numbers.

Table 2–13. Motor Headers Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
J5.3	Motor header 1 I/O pin	MAX_MOTOR_1_0	Variable VCCIO voltage (1.2-V to 3.3-V)	B1
	Motor header 1 I/O pin	MAX_MOTOR_1_1		B3
	Motor header 1 I/O pin	MAX_MOTOR_1_2		A2
	Motor header 1 I/O pin	MAX_MOTOR_1_3		A6
	Motor header 1 I/O pin	MAX_MOTOR_1_4		A4
	Motor header 1 I/O pin	MAX_MOTOR_1_5		A5
J5.2	Motor header 1 feedback signal A	MOTOR_1_FB_A		C7
J5.4	Motor header 1 feedback signal B	MOTOR_1_FB_B		C6
J5.6	Motor header 1 control signal	MOTOR_1_FB_CTRL		C5
J5.1	Power	VAR_VCCIO		—
J5.5	Ground	GND		—
J10.3	Motor header 2 I/O pin	MAX_MOTOR_2_0		A10
	Motor header 2 I/O pin	MAX_MOTOR_2_1		A15
	Motor header 2 I/O pin	MAX_MOTOR_2_2		A11
	Motor header 2 I/O pin	MAX_MOTOR_2_3		A13
	Motor header 2 I/O pin	MAX_MOTOR_2_4		A12
	Motor header 2 I/O pin	MAX_MOTOR_2_5		B16
J10.2	Motor header 2 feedback signal A	MOTOR_2_FB_A		D12
J10.4	Motor header 2 feedback signal B	MOTOR_2_FB_B		B12
J10.6	Motor header 2 control signal	MOTOR_2_FB_CTRL	Variable VCCIO voltage (1.2-V to 3.3-V)	E13
J10.1	Power	VA_VCCIO		—
J10.5	Ground	GND		—

Table 2–16 lists the motor headers component reference and the manufacturing information.

Table 2–14. Motor Headers Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J10	Surface mount terminal strip	Samtec	TSM-103-01-L-DV-TR	www.samtec.com
—	DC motor (30:1 Micro Metal Gearmotor) *(1)*	Cytron Technologies	MO-SPG-10-30K	www.cytron.com.my
—	DC motor encoder (encoder for Pololu wheel 42×19 mm) *(1)*	Pololu	SN-EN-PW4219	www.cytron.com.my

Note to Table 2–14:

(1) This component is a compatible unit which can be used on the development board. The MAX V CPLD development kit does not include this component.

General User Input/Output

This section describes the user I/O interface to the CPLD, including the push-buttons and status LEDs.

User-Defined Push-Button Switches

The development board includes two user-defined push-button switches. Board references S1 (USER_PB1) and S2 (USER_PB0) are push-button switches that allow you to interact with the MAX V CPLD device. There is no board-specific function for these user-defined push-button switches.

Table 2–15 lists the user-defined push-button switch schematic signal names and their corresponding MAX V CPLD device pin numbers.

Table 2–15. User-Defined Push-Button Switch Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
S2	User-defined push-button switch. When the switch is pressed and held down, the device pin is set to logic 0; when the switch is released, the device pin is set to logic 1.	USER_PB0	3.3-V	M9
S1		USER_PB1		R3

Table 2–16 lists the user-defined push-button switch component reference and the manufacturing information.

Table 2–16. User-Defined Push-Button Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S1, S2	Push-button switches	Dawning Precision Co., Ltd.	TS-A02SA-2-S100	www.dawning2.com.tw

User-Defined LEDs

The development board includes two general purpose LEDs. Board references D7 (USER_LED1) and D8 (USER_LED0) are user-defined LEDs which allow status and debugging signals to be driven to the LEDs from the CPLD designs loaded into the MAX V CPLD device. There is no board-specific function for these LEDs.

Table 2–17 lists the user-defined LED schematic signal names and their corresponding MAX V CPLD pin numbers.

Table 2–17. User-Defined LED Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
D8	User-defined LEDs. Driving a logic 0 on the I/O port illuminates the LED. Driving a logic 1 on the I/O port turns off the LED.	USER_LED0	3.3-V	P4
D7		USER_LED1		R1

Table 2–18 lists the user-defined LED component reference and the manufacturing information.

Table 2–18. User-Defined LED Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D7, D8	Green LEDs	Lumex, Inc.	SML-LX1206GC-TR	www.lumex.com

Off-Chip EEPROM

This section describes the board's EEPROM interface support and also their signal names, types, and connectivity relative to the MAX V CPLD device. The board include footprints for you to mount the following EEPROM device:

- I²C EEPROM
- SPI EEPROM

The MAX V CPLD development board only provide the EEPROM device footprints. However, the board test system EEPROM function is developed based on the EEPROM components described in this section.

I²C EEPROM

Board reference U6 is a footprint to mount an I²C EEPROM device onto the development board.

Table 2–19 lists the I²C EEPROM device pin assignments, signal names, and functions. The signal names and types are relative to the MAX V CPLD device in terms of I/O setting and direction.

Table 2–19. I²C EEPROM Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
U6.1	Clock to synchronize the data transfer to and from the device.	I2C_PROM_SCL	3.3-V	T13
U6.2	Bidirectional serial data pin to transfer addresses and data into and out of the device.	I2C_PROM_SDA		R13
U6.5	Write-protect pin. ■ Tied to V_{ss}: Normal operation (read or write to the entire memory of 000-3FF). ■ Tied to V_{cc}: Write operation disabled (the entire memory is write-protected). Read operation is not affected.	I2C_PROM_WP		—

Table 2–20 lists the I²C EEPROM component reference and manufacturing information.

Table 2–20. I²C EEPROM Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U6	8-Kbit EEPROM, 256 × 8-bit memory *(1)*	Microchip	24LC08BT-I/OT	www.microchip.com

Note to Table 2–20:

(1) This component is a compatible unit which can be used on the development board. The MAX V CPLD development kit does not include this component.

SPI EEPROM

Board reference U8 is a footprint to mount a SPI EEPROM device onto the development board.

Table 2–21 lists the SPI EEPROM pin assignments, signal names, and functions. The signal names and types are relative to the MAX V CPLD device in terms of I/O setting and direction.

Table 2–21. SPI EEPROM Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
U8.1	SPI chip select signal	SPI_CSn	3.3-V	R14
U8.2	SPI data in signal (master-in-slave-out)	SPI_MISO		T15
U8.5	SPI data out signal (master-out-slave-in)	SPI_MOSI		P13
U8.6	SPI clock signal	SPI_SCK		R16

Table 2–22 lists the SPI EEPROM component reference and manufacturing information.

Table 2–22. SPI EEPROM Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U8	256-Kbit serial EEPROM *(1)*	Microchip	25LC256-I/ST	www.microchip.com

Note to Table 2–22:

(1) This component is a compatible unit which can be used on the development board. The MAX V CPLD development kit does not include this component.

Power Supply

The development board is powered up through a USB cable. The blue LED illuminates when the board is powered up. Alternatively, you can also power-up the board by connecting three 1.5-V batteries in series (to obtain 4.5 V) through connectors BATT+ and BATT-.

Once you plug the USB cable into the board's USB connector and connect the other end of the cable to a PC USB slot, the board disconnects the battery supply and switch over to obtain power supply from the USB cable.

Table 2–23 lists the power rails.

Table 2–23. Power Rails

Rail	Schematic Signal Name	Voltage (V)	Device Pin	Description
1	1.8_VCCINT	1.8	VCCINT	CPLD core voltage
2	VAR_VCCIO	1.2 – 3.3	VCCIO	CPLD I/O bank 2 variable voltage
3	3.3V	3.3	VCCIO	Power for I/O bank 1 and EEPROM
4	5V	5.0	5V_USB	Power-up USB peripheral

Table 2–24 lists the power rail component reference and manufacturing information.

Table 2–24. Power Supply Rail Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U7	400 mA, 2.25 MHz synchronous step-down DC/DC converter	Linear Technology	LTC3670	www.linear.com

Statement of China-RoHS Compliance

Table 2–25 lists hazardous substances included with the kit.

Table 2–25. Table of Hazardous Substances' Name and Concentration *Notes (1), (2)*

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
MAX V CPLD development board	X*	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0

Notes to Table 2–25:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
September 2015	1.1	Corrects descriptions of J7.2, J7.3, J7.6, and J7.7 in "GPIO Header B Schematic Signal Names and Functions" on page 2–9.
January 2011	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.